UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,078	12/31/2003	Young-Jae Cho	51876P567	1882

8791 7590 04/11/2005

BLAKELY SOKOLOFF TAYLOR & ZAFMAN
12400 WILSHIRE BOULEVARD
SEVENTH FLOOR
LOS ANGELES, CA 90025-1030

EXAMINER	
WAMSLEY, PATRICK G	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/750,078	CHO ET AL.	
	Examiner	Art Unit	
	Patrick G. Wamsley	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 20-24* is/are rejected.

7)☐ Claim(s) *4-19 and 25-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

The disclosure is objected to because of the following informalities:

Page 2, line 26: Change "operational step" to -- operation --.

Page 8, line 14: Change "two pair of a resistor and a capacitor" to -- two pairs of resistors and capacitors --.

Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claims 3, 6, 11, 17, 19, 20, 24, 26,28 are objected to because of the following informalities:

Claim 3, line 4: Change "removing a noise" to -- removing noise --.

Claim 6, line 5: Change "voltage shifting" to -- voltage dividing --.

Claim 11, line 3: Change "voltage shifting" to -- voltage dividing --.

Claim 17, line 3: Change "first" to -- second --.

Claim 19, line 4: Change "first resistor" to -- second resistor --.

Claim 20, line 2: Change "filter is" to -- filters are --.

Claim 24, line 4: Change "removing a noise" to -- removing noise --.

Claim 26, line 6: Change "voltage shifting" to -- voltage dividing --.

Claim 28, line 2: Change "filter is" to -- filters are --.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 22 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 6,486,820 to Allworth et al, hereafter Allworth.

Allworth discloses a pipeline analog-to-digital converter, hereafter ADC, implemented in one chip [CMOS integrated circuit: col. 1, lines 32-33], comprising an on-chip reference voltage generator [417: Fig. 4] for generating reference voltages [Figure 8A]; and a conversion means [415: Fig. 4] for converting the inputted analog signal [INPUT: Fig. 4] into a digital signal [OUTPUT BITS: Fig. 4] by using the reference voltages. Claim 22 restates these apparatus limitations in means plus function format.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 2 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allworth in view of U.S. Patent 5,280,200 to Tarng, hereafter Tarng.

Unlike claims 2 and 23, Allworth lacks a voltage level shifter. In contrast, as depicted in Fig. 4A, Tarng couples a reference voltage generator to a level shift circuit [col. 4, line 13]. At the time of the invention, it would have been obvious to one of ordinary skill in the art to have applied Tarng's level shift teachings to Allworth's reference voltage generator. The motivation would have been to reduce the impact of the power source, as suggested by Tarng [col. 7, lines 49-53].

Claims 3, 20, 21, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Allworth in view of U.S. Patent 6,657,484 to Bosshart, hereafter Bosshart.

Unlike claims 3 and 24, Allworth is silent regarding filters. In contrast, as depicted in Fig. 3, Bosshart uses filters with an integrated chip [abstract, line 3-5]. At the time of the invention, it would have been obvious to one of ordinary skill in the art to have applied Bosshart's filter teachings to Allworth's reference voltage generator. The motivation would have been to reduce resonance on Allworth's integrated circuit [col. 1, lines 36-49]. For claim 20, Bosshart provides a plurality of multi-stage RC filters [col. 1, lines 59-60]. For claim 21, Bosshart indicates that the gate capacitance of CMOS transistors can be used in a filter [col. 7, lines 19-39]. Because the gate capacitance of the CMOS transistor would act as one plate of the capacitor, the source, drain, and body of the transistor would inherently serve as the other plate.

Allowable Subject Matter

Claims 4-19 and 25-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: the references of record neither reveal nor render obvious an on-chip reference voltage generator for an ADC having an initial voltage generator coupled to a level shifter in the recited manner.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. U.S. Patent 6,867,639 to Chun shows a voltage generator having differential amplifiers [DA1/DA2] and MOS transistors [MP12/MN12]. U.S. Patent 6,570,367 to Bartenschlager et al describes a voltage generator having a voltage divider. U.S. Patent 6,542,026 to Wu et al discloses an on-chip reference voltage generator. U.S. Patent 6,281,828 to Kimura et al provides a reference voltage generator [3, Figs. 11A & 11B] for an ADC. U.S. Patent 5,886,657 to Ahuja provides a reference voltage circuit for a DAC. U.S. Patent 5,642,072 to Miyamoto et al shows a voltage generator having a limiter circuit. U.S. Patent 5,721,702 to Briner provides a reference voltage generator having a differential amplifier [42]. U.S. Patent 5,399,960 to Gross shows a reference voltage generator with an active filter. U.S. Patent 5,280,455 to Kanaishi furnishes first [31] and second [32] reference voltage generators.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patrick G. Wamsley whose telephone number is (571) 272-1814. The official facsimile number is (703) 872-9306. An alternate facsimile number, (571) 273-1814, should only be used for unofficial documents.

Patrick G. Wamsley
April 6, 2005